4.5.7 – 168 PIN REGISTERED SDRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:

—64 BIT without PARITY

—72 BIT for PARITY CODES

—80 BIT for ECC CODES

CONFIGURATION—12 Different Configurations are defined using various combinationa of X4 & X8 memories including 1 & 2 bank configurations.

LOGIC FEATURES—The modules contain a “SERIAL PRESENCE DETECT” feature that supplies encoded values that define the storage capacity, configuration, data word configuration, refresh mode, speed of the module and other characteristics and attributes of the module.

—All logic, control, and address inputs are buffered by an on–module register.

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS—Figs. 4.5.7–A, & 4.5.7–B,

SPD TABLE & INFORMATION—Fig. 4.5.7–C

KEYING METHODOLOGY—Fig. 4.5.7–D

PINOUT COMPARISON DRAM & SDRAM DIMM—Fig. 4.5.7–E

SDRAM DIMM REGISTER CLOCK LOADING—Fig. 4.5.7–F

SDRAM DIMM CLOCK LOADING—Fig. 4.5.7–G

SDRAM DIMM CLOCK WIRING—Fig. 4.5.7–H

SDRAM DIMM Block Diagrams General Information/Recommended Design Guidelines—Fig. 4.5.7–I

CONFIGURATION BLOCK DIAGRAMS—Figs. 4.5.7–J through 4.5.7–X

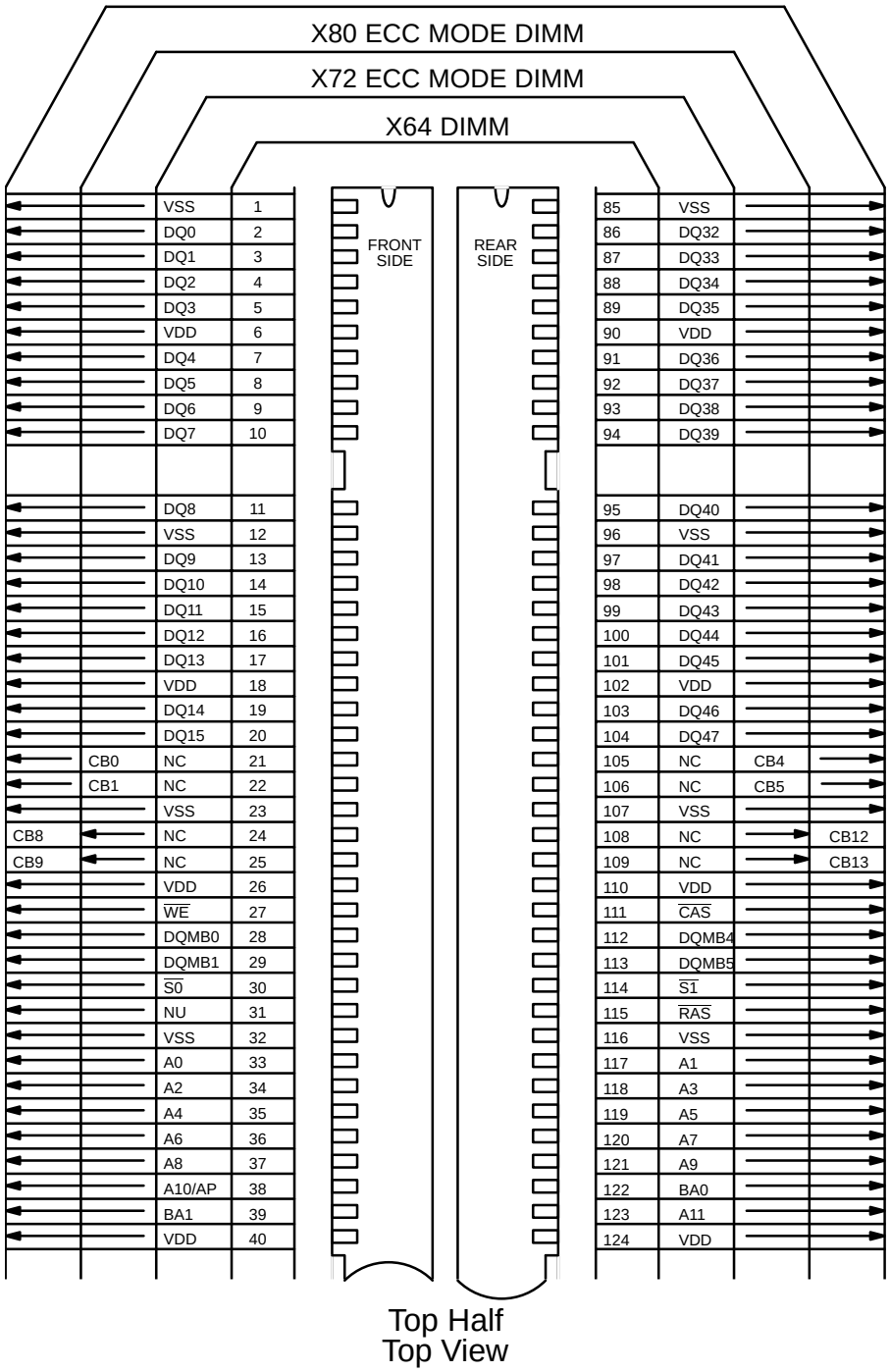
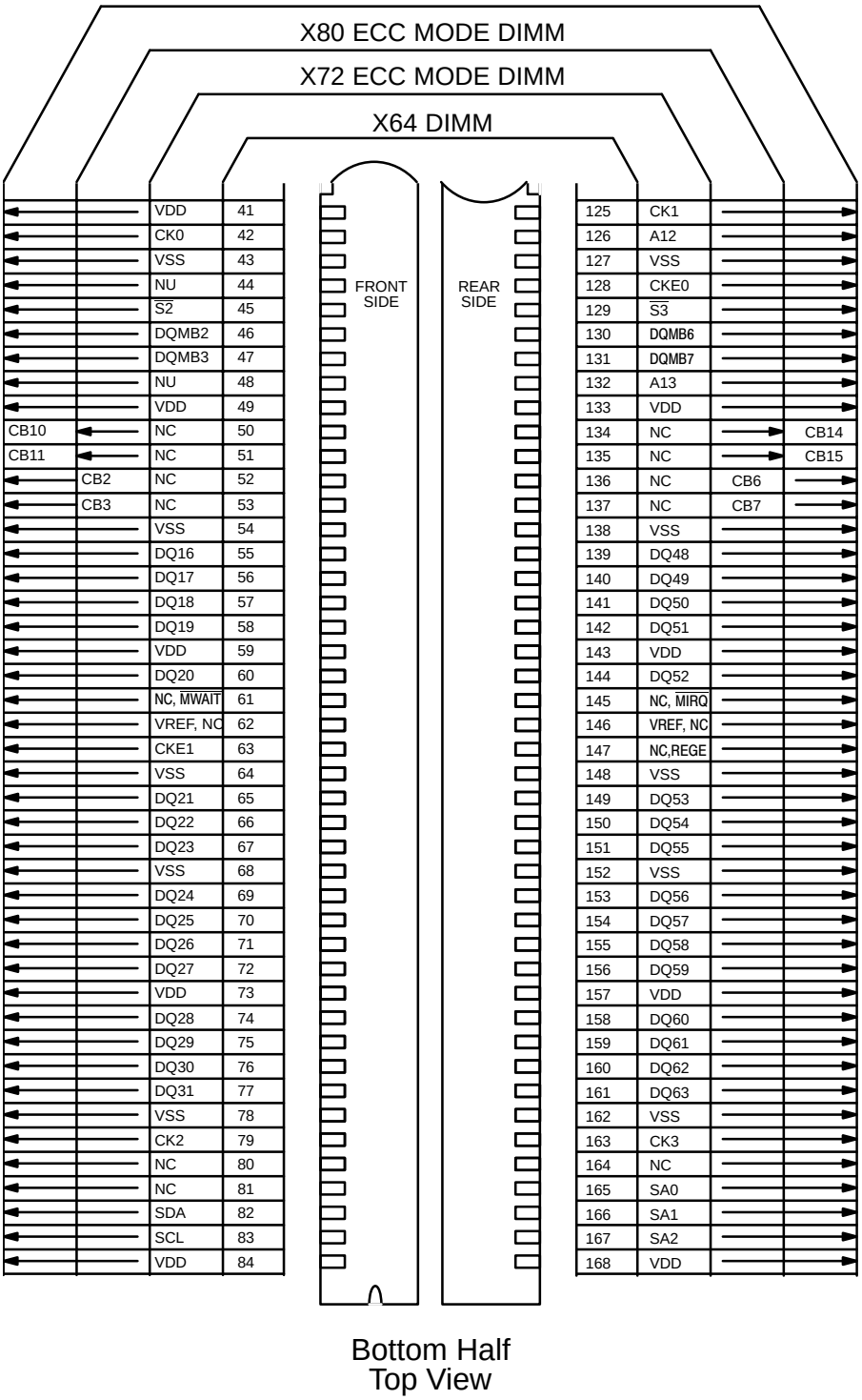


FIGURE 4.5.7–A

168 PIN, 64, 72, or 80 BIT REGISTERED SDRAM DIMM PINOUT, TOP HALF



Bottom Half
Top View

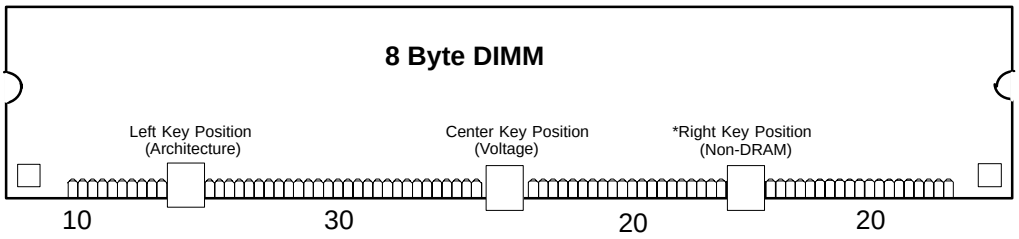
FIGURE 4.5.7–B
168 PIN, 64, 72, or 80 BIT REGISTERED SDRAM DIMM PINOUT, BOTTOM HALF

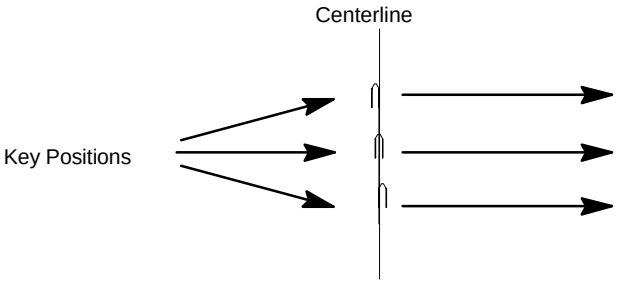
Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	# Bank Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	# Bank Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.
4M x 64/72/80	4M x 4	1	11	10						
8M x 64/72/80	4M x 4	1	11	10						
16M x 64/72/80	16M x 4	2	12	10	1	13	10			
32M x 64/72/80	16M x 4	2	12	10	1	13	10			
64M x 64/72/80	64M x 4	2	13	11						
128M x 64/72/80	64M x 4	2	13	11						
2M x 64/72/80	2M x 8	1	11	9						
4M x 64/72/80	2M x 8	1	11	9						
8M x 64/72/80	8M x 8	2	12	9	1	13	9			
16M x 64/72/80	8M x 8	2	12	9	1	13	9			
32M x 64/72/80	32M x 8	2	13	10						
64M x 64/72/80	32M x 8	2	13	10						
(Note: All options possible with SDRAM standards are shown)										

b. Allowable configurations: (Byte 11)
   - x64 (Non-parity, Byte controls)
   - x72 (ECC-optimized, Byte controls)
   - x80 (ECC-optimized, Byte controls)

c. All other bytes (in 0-31 address range) must be coded to reflect the DIMM functional and performance characteristics.

Figure 4.5.7–C
168 Pin REGISTERED SDRAM DIMM SPD ASSIGNMENTS





Left Key Position	Center Key	*Right Key
RFU	5V	No Key
**1st GENERATION 168 PIN DIMM	3.3V	No Key
***2nd GENERATION 168 PIN DIMM	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.
** 1st Generation: Initial 168P DIMM standard described in Sec. 4.5.1. This standard included buffering on all inputs except RAS and DQs as well as Parallel Presence Detect (PD).
*** 2nd Generation: Originally described as “Unbuffered” DRAM & SDRAM. DIMMs, these DIMMs have Serial PDs, and both DRAM & SDRAM versions.

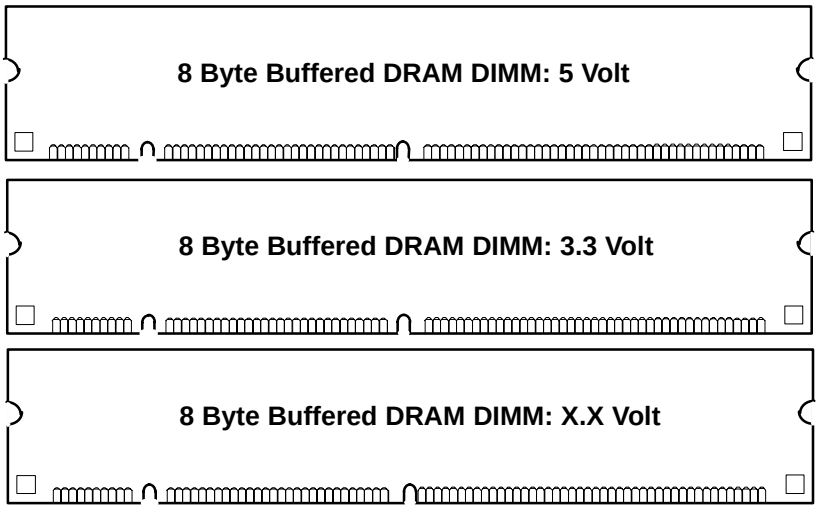


FIGURE 4.5.7–D
168 Pin REGISTERED SDRAM DIMM Keying Methodology

Pin #	UN–BUFF. DRAM DIMM	REG. SDRAM DIMM
28	$\overline{CAS0}$	DQMB0
29	$\overline{CAS1}$	DQMB1
30	$\overline{RAS0}$	$\overline{S0}$
31	$\overline{OE0}$	NU
39	A12	BA1
42	NU	CK0
44	$\overline{OE2}$	$\overline{NU}$
45	$\overline{RAS2}$	$\overline{S2}$
46	$\overline{CAS2}$	DQMB2
47	$\overline{CAS3}$	DQMB3
48	$\overline{WE2}$	NU
62	NU	V_{REF}, NC
63	NC	CKE1
79	NC	CK2
111	$\overline{NU}$	$\overline{CAS}$
112	$\overline{CAS4}$	DQMB4
113	$\overline{CAS5}$	DQMB5
114	$\overline{RAS1}$	$\overline{S1}$
115	NU	$\overline{RAS}$
122	A11	BA0
123	A13	A11
125	NU	CK1
126	NU	A12
128	$\overline{NU}$	$\overline{CKE0}$
129	$\overline{RAS3}$	$\overline{S3}$
130	$\overline{CAS6}$	DQMB6
131	CAS7	DQMB7
132	NU	A13
146	NU	NC, VREF
147	NC	NC, REGE
163	NC	CK3

Notes:
1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. Pin assignments for Unbuffered and Registered 168 Pin SDRAM DIMMs are identical

FIGURE 4.5.7–E
Pinout Comparison, 168 Pin Unbuff. DRAM & Reg. SDRAM DIMM

	1 Bank DIMM, x4 SDRAMS	2 Bank DIMM, x4 SDRAMS	1 Bank DIMM, x8 SDRAMS	2 Bank DIMM, x8 SDRAMS
Addr. (A0 - AN)	20 SDRAMS	20 SDRAMS	10 SDRAMS	20 SDRAMS
Bank Addr. (BA0 - BAN)	20 SDRAMS	20 SDRAMS	10 SDRAMS	20 SDRAMS
Select ($\overline{S0}$ - $\overline{S3}$)	10 SDRAMS	10 SDRAMS	5 SDRAMS	10 SDRAMS
Byte Control (DQMB0 - DQMB7)	2-3 SDRAMS	4-6 SDRAMS	1-2 SDRAMS	4-6 SDRAMS
Clock Enable (CKE0 - CKE1)	10 SDRAMS	10 SDRAMS	10 SDRAMS	10 SDRAMS
RAS	20 SDRAMS	20 SDRAMS	10 SDRAMS	20 SDRAMS
CAS	20 SDRAMS	20 SDRAMS	10 SDRAMS	20 SDRAMS
WE	20 SDRAMS	20 SDRAMS	10 SDRAMS	20 SDRAMS

Notes:

1. Recommended register loading, as shown in above table, is identical to the loading found on a 1 bank (x4) Unbuffered SDRAM DIMM.
2. To achieve specified loading, some DIMM configurations will require >1 register output for a given input.

Figure 4.5.7–F
168 Pin UNBUFFERED SDRAM DIMM REGISTER LOADING

SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
x4	1	16	* PLL	*	*	*
x4	2	32	* PLL	*	*	*
x8	1	8	* PLL	*	*	*
x8	2	16	* PLL	*	*	*

SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
x4	1	18	* PLL	*	*	*
x4	2	36	* PLL	*	*	*
x8	1	9	* PLL	*	*	*
x8	2	18	* PLL	*	*	*

SDRAM Data Width	# of Banks on DIMM	Total # SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
x4	1	20	* PLL	*	*	*
x4	2	40	* PLL	*	*	*
x8	1	10	* PLL	*	*	*
x8	2	20	* PLL	*	*	*

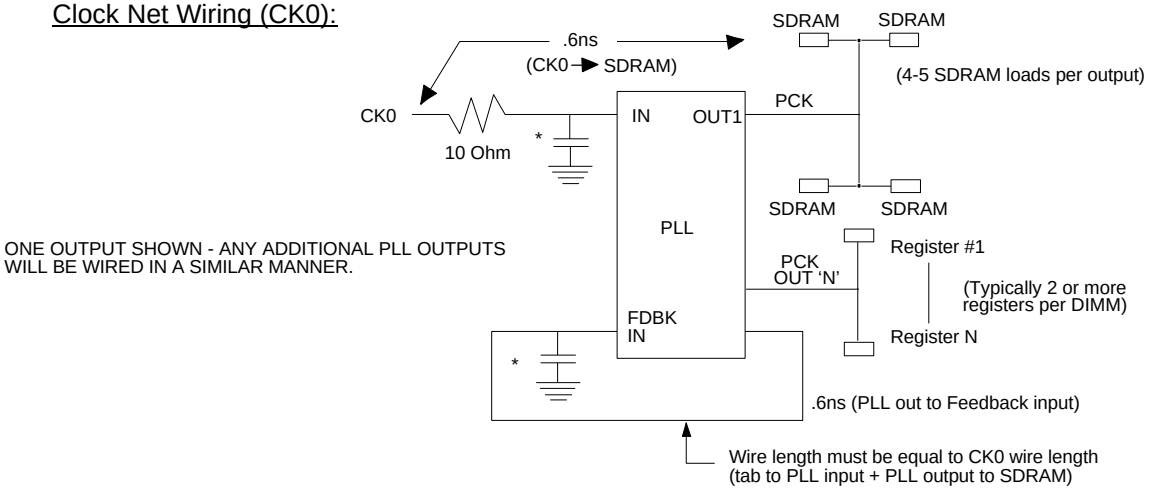
Notes:

* Add padding capacitance per clock wiring detail - Each PLL output will have no more than 4 SDRAM loads or equivalent “register” loads.

- CK1 - CK3 are not used on this DIMM family, but are padded to represent typical clock wiring and SDRAM loads. This permits clock inputs to be “dotted” at the next level of assembly.

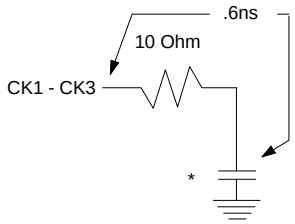
Figure 4.5.7–G
168 Pin REGISTERED SDRAM DIMM CLOCK LOADING

Clock Net Wiring (CK0):



0 LOAD NETS:

(CK1 - CK3)



TARGET CLOCK (CK) SPECIFICATION:

1. THE CK INPUTS SHOULD HAVE A NOMINAL FLIGHT-TIME OF .6ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PADDING CAPACITOR). (EG: THIS IS EQUIVALENT TO APPROXIMATELY 3" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2. PLL OUTPUTS (PCK) MUST BE WIRED TO ASSURE TRACKING WITHIN +/- 100PS AT THE LOAD (SDRAM, REGISTER OR PADDING CAPACITOR).

.

* Add padding capacitance to approximate 4 SDRAM loads (total).

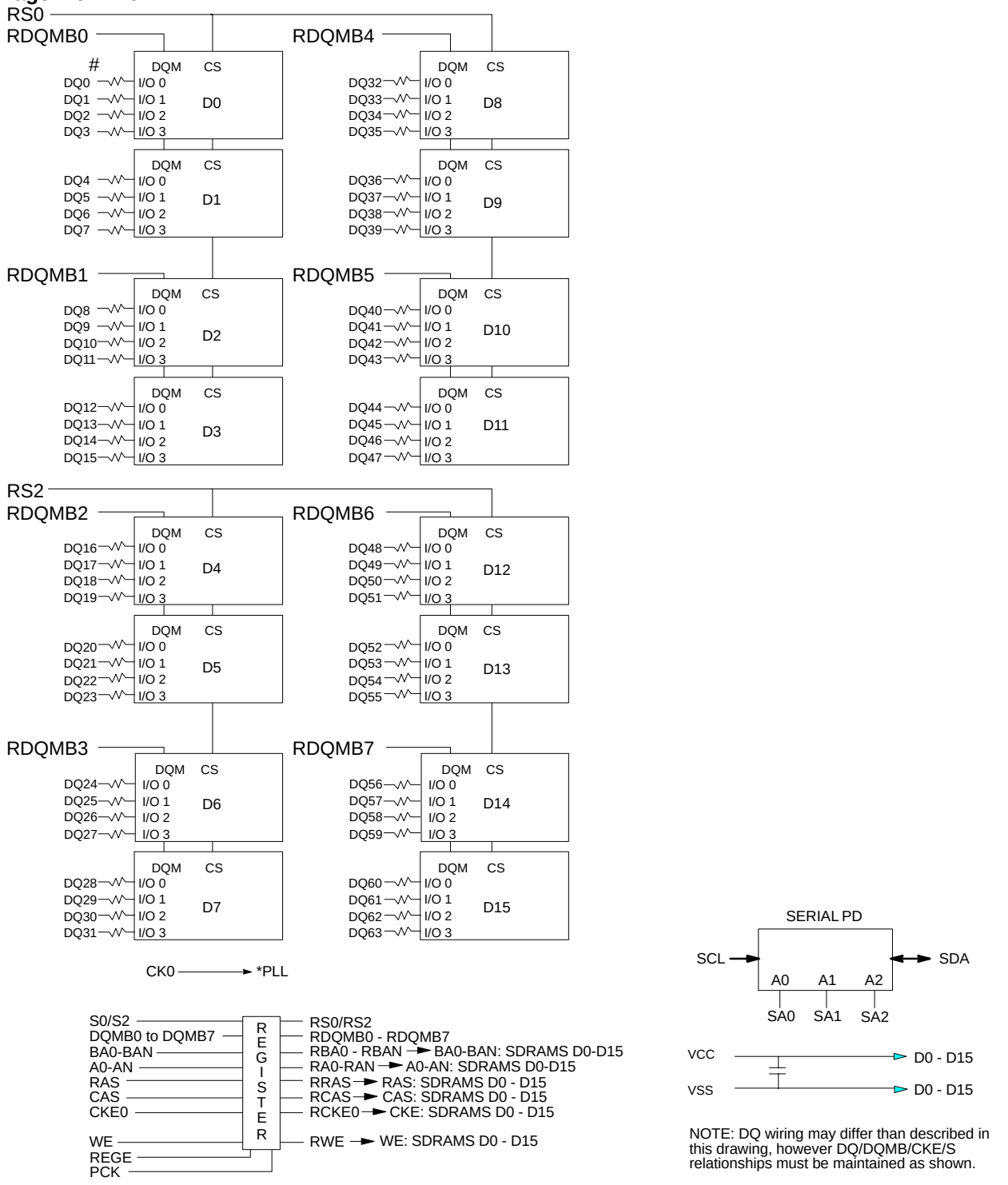
Figure 4.5.7–H
168 Pin REGISTERED SDRAM DIMM CLOCK WIRING

- **Clocks:**
  - **Clock Structure:** Refer to tables and diagrams (before block diagrams) for detailed clock design guidelines. Clock wires should be placed on an internal wiring layer.
  - **Clock Skew/Jitter:** Total skew/jitter should not exceed +/- 500ps (at SDRAM).

- **Registers:**
  - Refer to register wiring information (after block diagrams) for detailed design information.
  - Additional Recommendations:
    - Registers should include a flow-through (buffer mode) to be in full compliance with JEDEC Standard. Pin 147 is defined as REGE (Register Enable) mode.
    - Register Clock-to-Q delay should be minimized.
  - Block Diagrams show only a simplified structure for registers - multiple outputs may be required to meet loading recommendations (see register loading table).

- **Misc:**
  - Data (DQ, CB) net lengths should be minimized. Wire lengths should not exceed 1.5” (tab to furthest SDRAM device)
  - Board impedance should be 65 ohms +/- 15% for signal layers. A cross section of S-P-S-S-P-S is recommended.
  - Diagrams for x64, x72 (x4, x8) and x80 DIMMs follow.

Figure 4.5.7–I
168 Pin REGISTERED SDRAM DIMM Block Diagrams
General Information/Recommended Design Guidelines

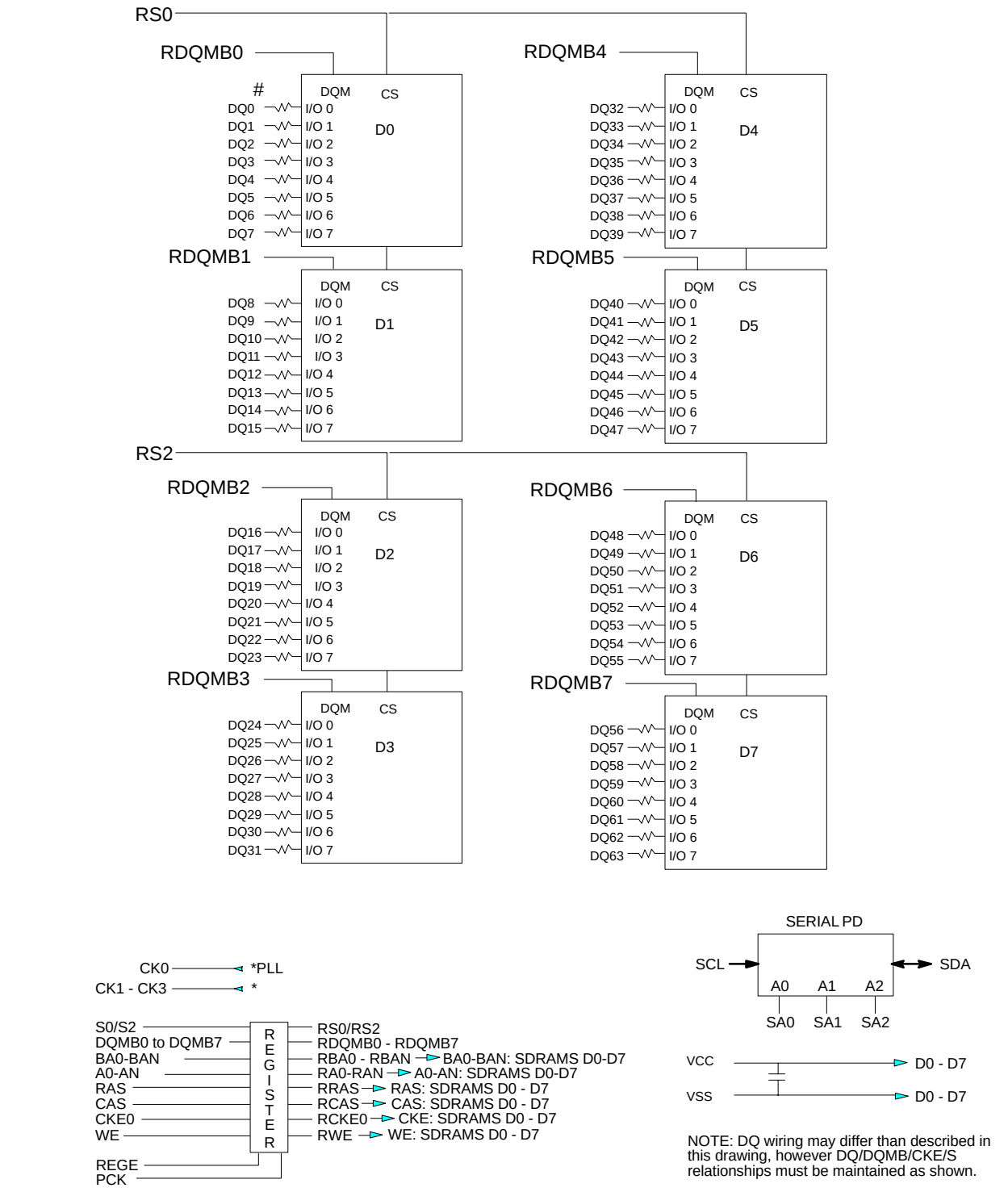


NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

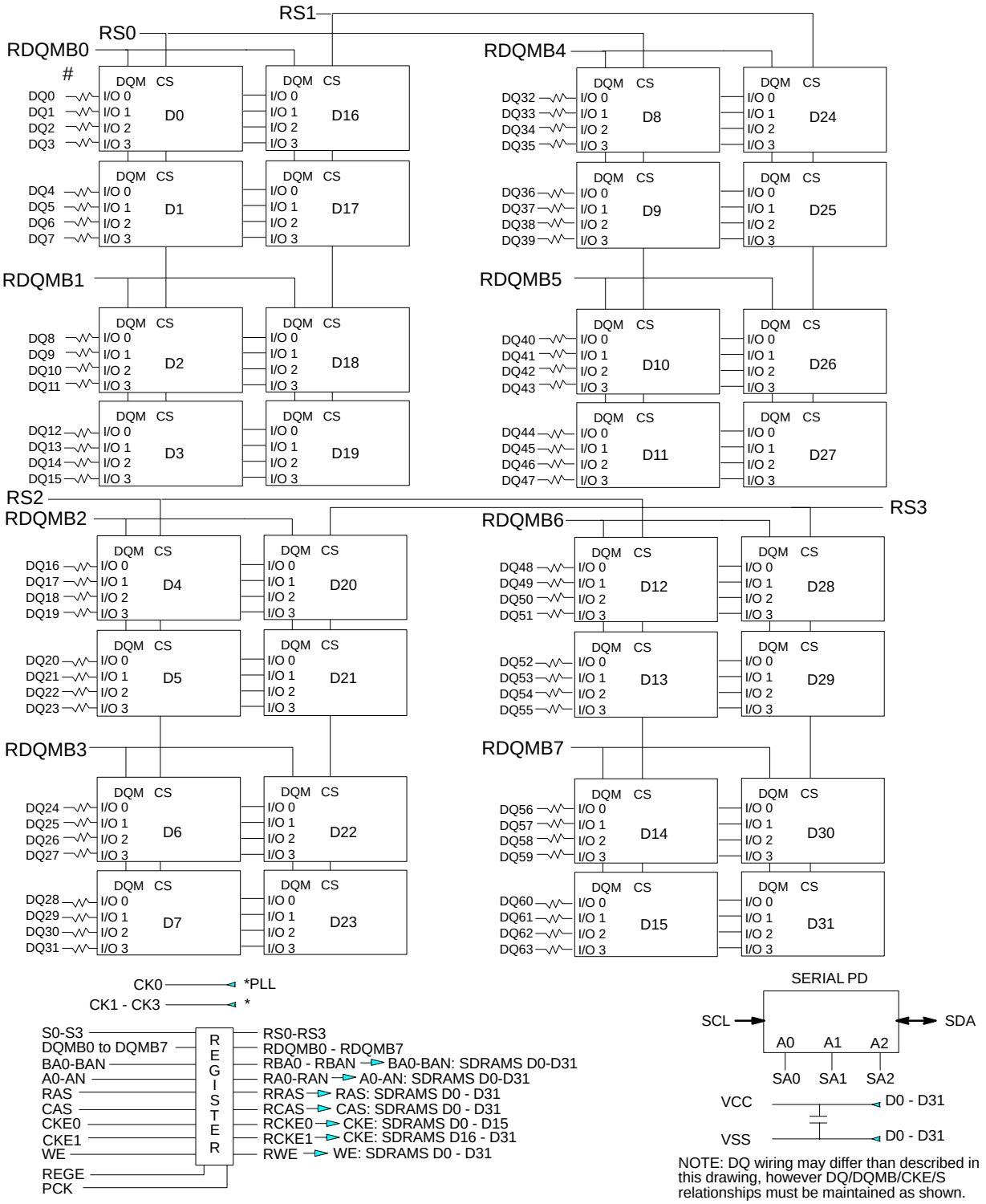
Figure 4.5.7–J
X64 REGISTERED SDRAM DIMM, 1 Bank with X4 SDRAMs, 1 CK



* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.7–K
X64 REGISTERED SDRAM DIMM, 1 Bank with X8 SDRAMs



* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.7–L
X64 REGISTERED SDRAM DIMM, 2 Bank with X4 SDRAMs

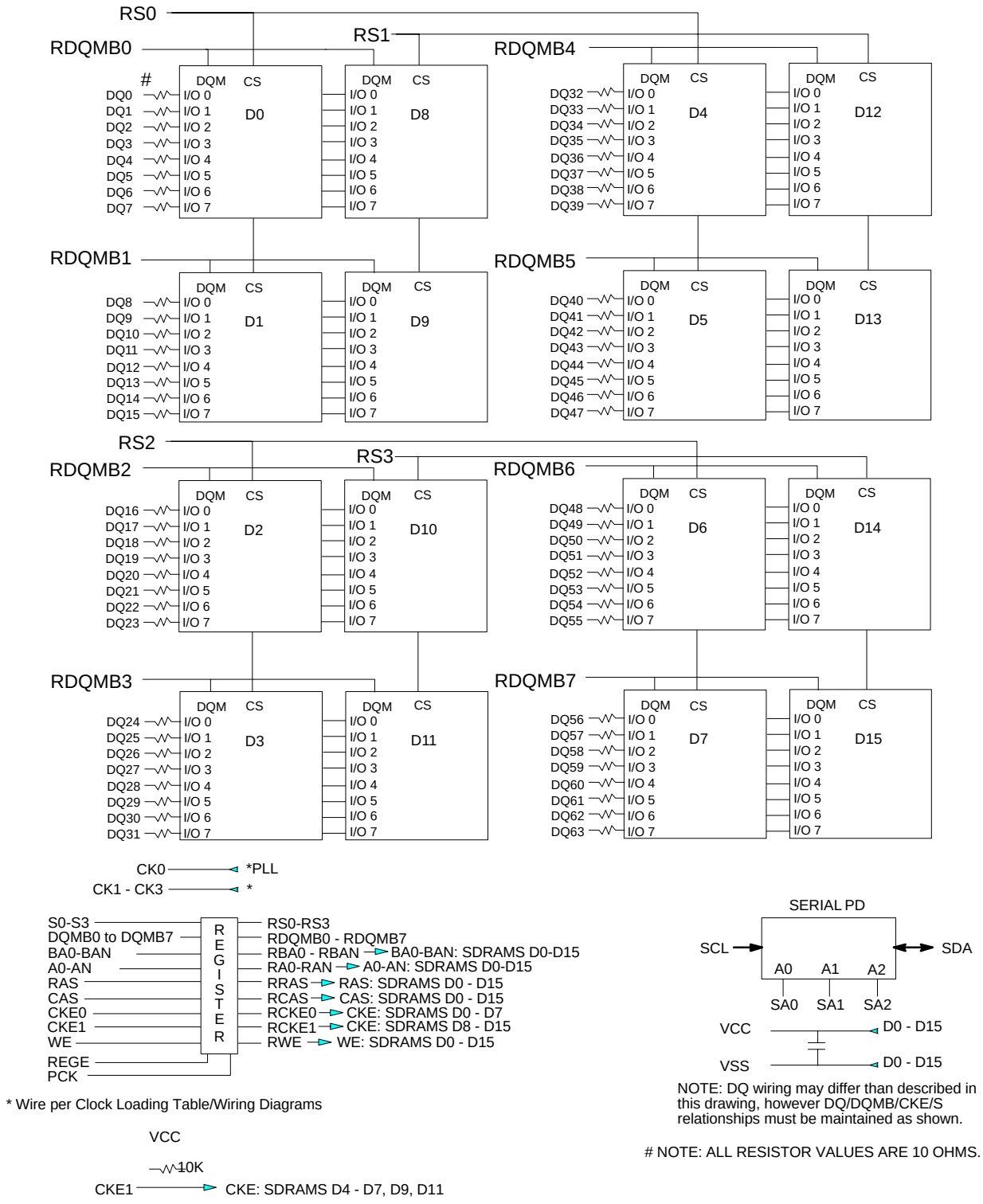
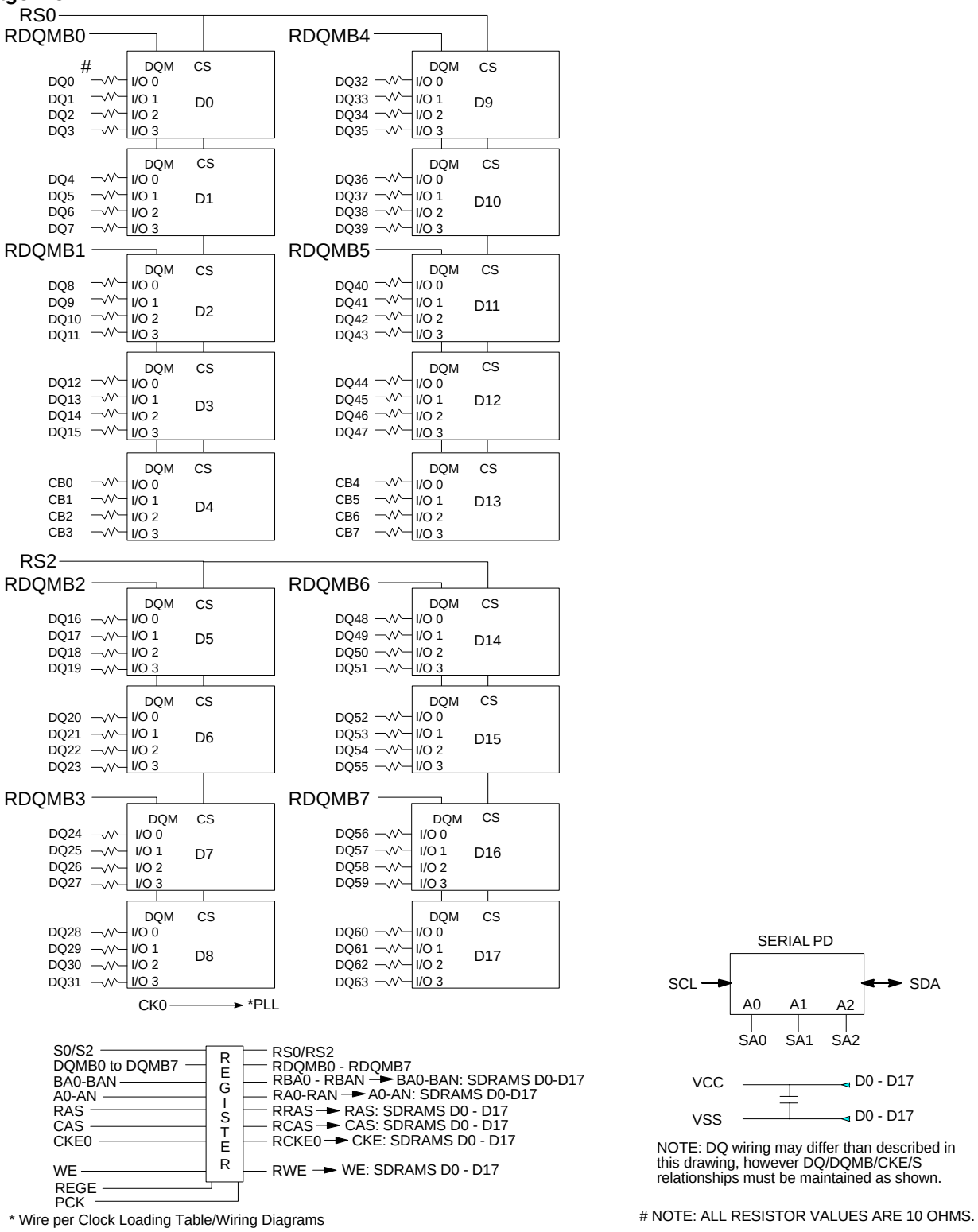


Figure 4.5.7–M
X64 REGISTERED SDRAM DIMM, 2 Bank with X8 SDRAMs



* Wire per Clock Loading Table/Wiring Diagrams

NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.7–N
X72 ECC REGISTERED SDRAM DIMM, 1 Banks with X4 SDRAMs, 1 CK

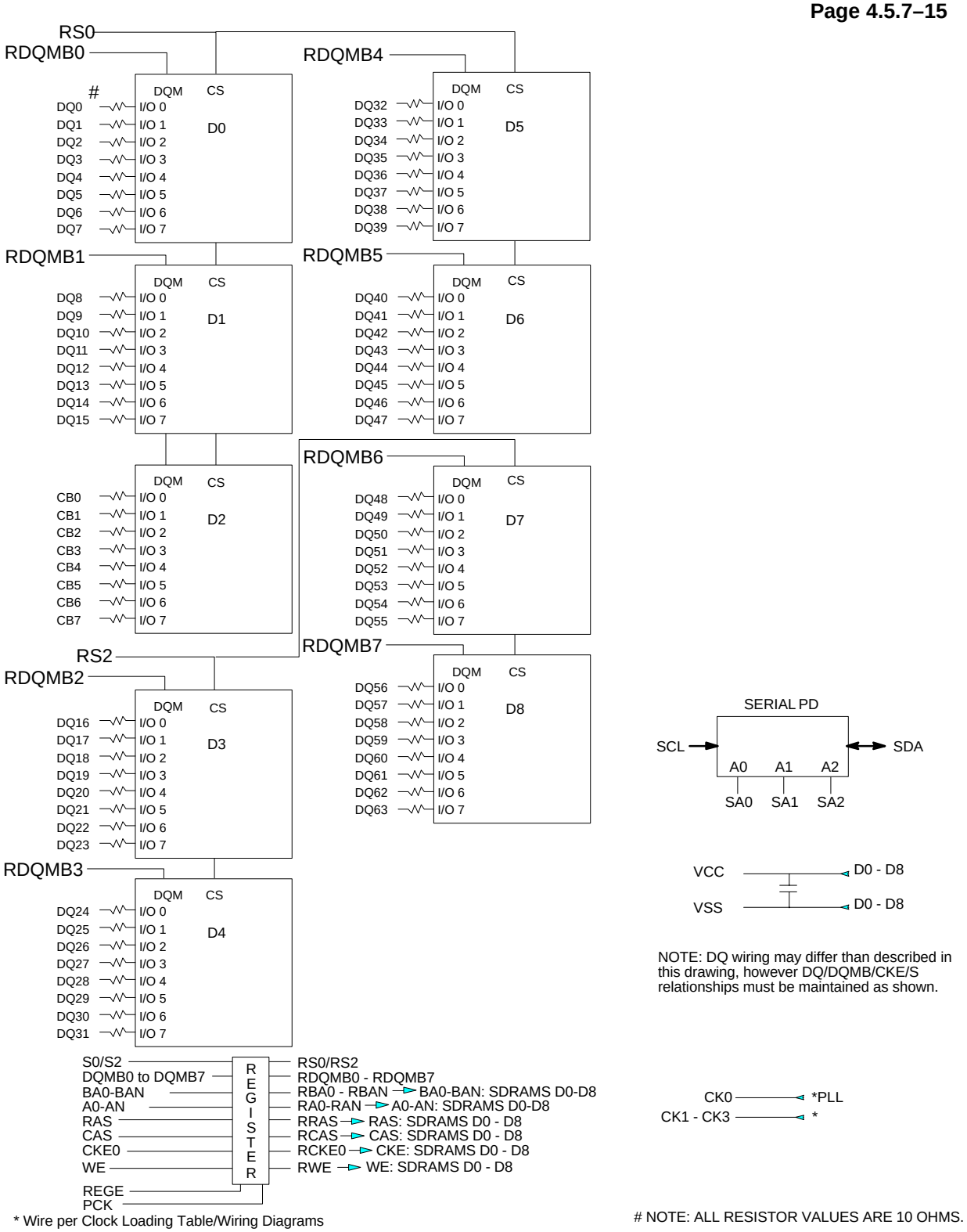
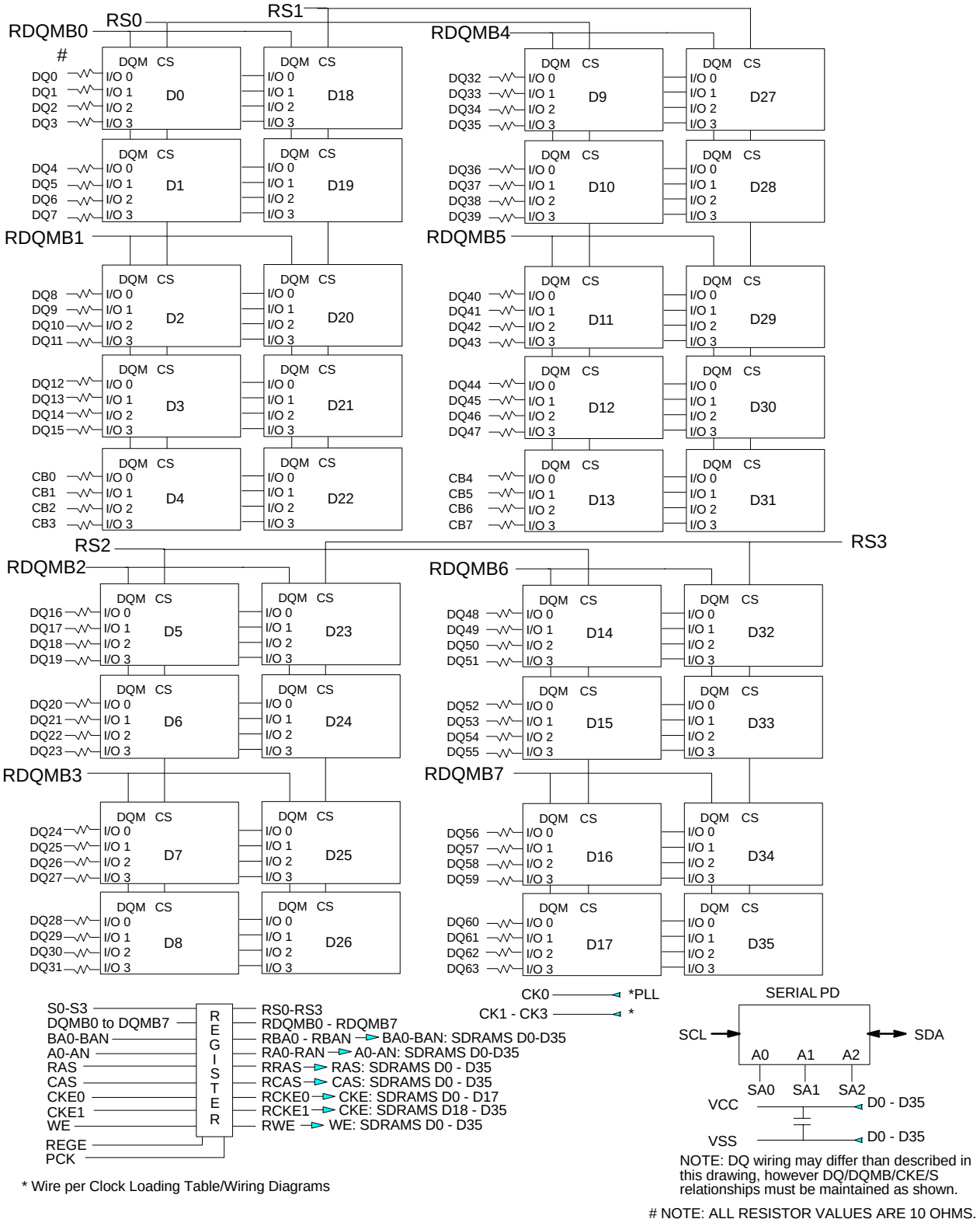


Figure 4.5.7–O
X72 ECC REGISTERED SDRAM DIMM, 1 Banks with X8 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.7–P
X72 ECC REGISTERED SDRAM DIMM, 2 Bank with X4 SDRAMs

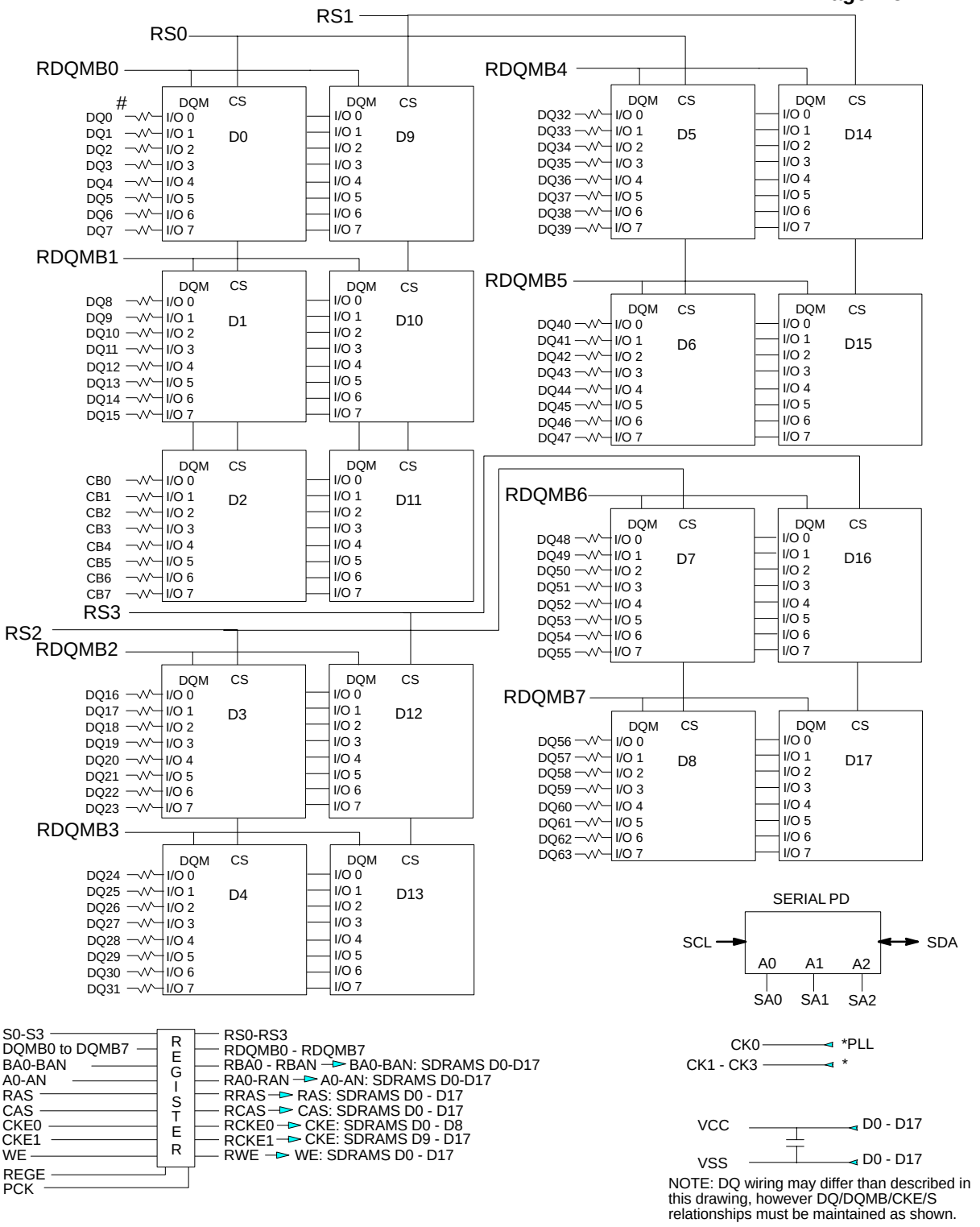


Figure 4.5.7–Q
X72 ECC REGISTERED SDRAM DIMM, 2 Banks with X8 SDRAMs

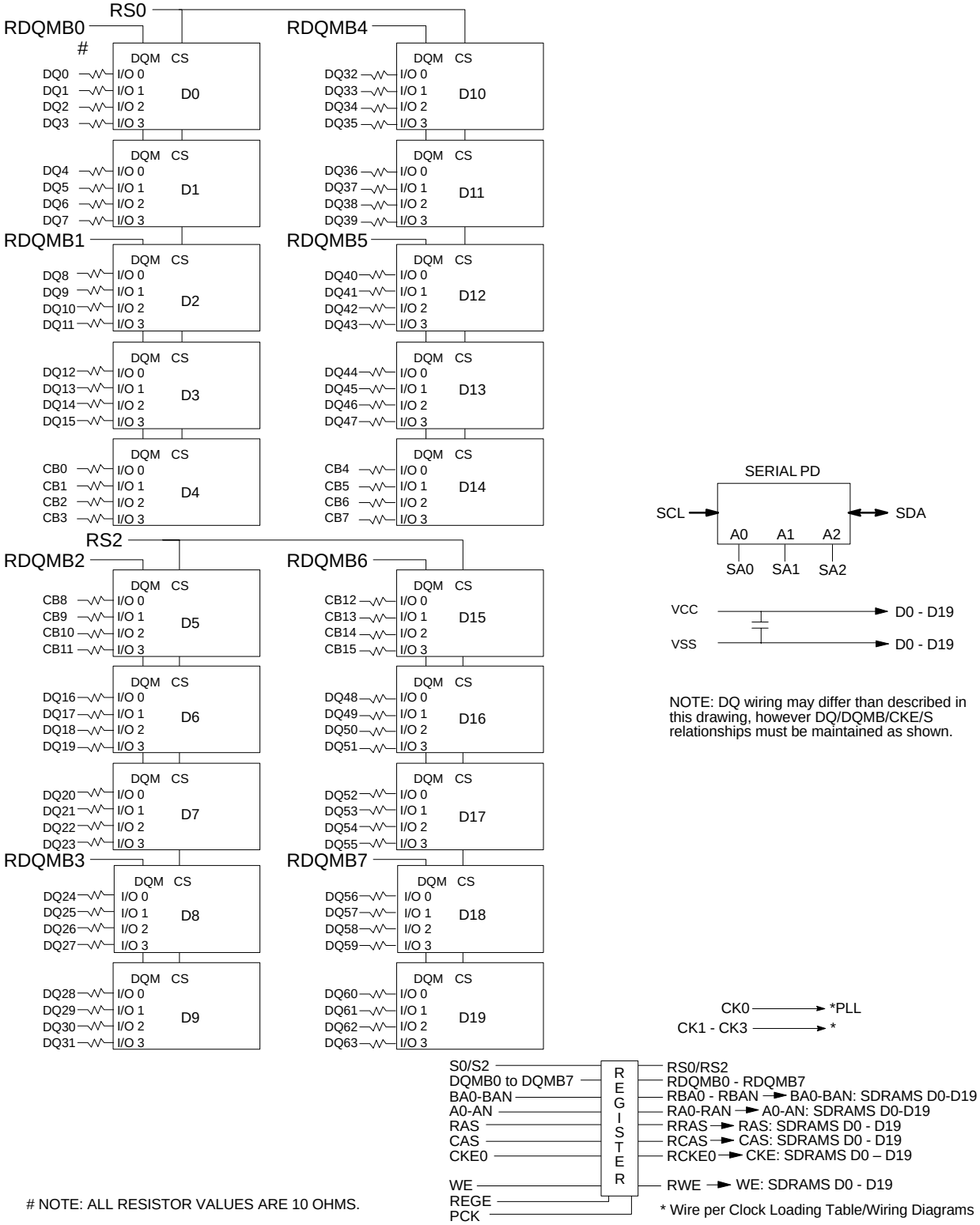


Figure 4.5.7–R
X80 REGISTERED SDRAM DIMM, 1 Bank with X4 SDRAMs, 1 CK

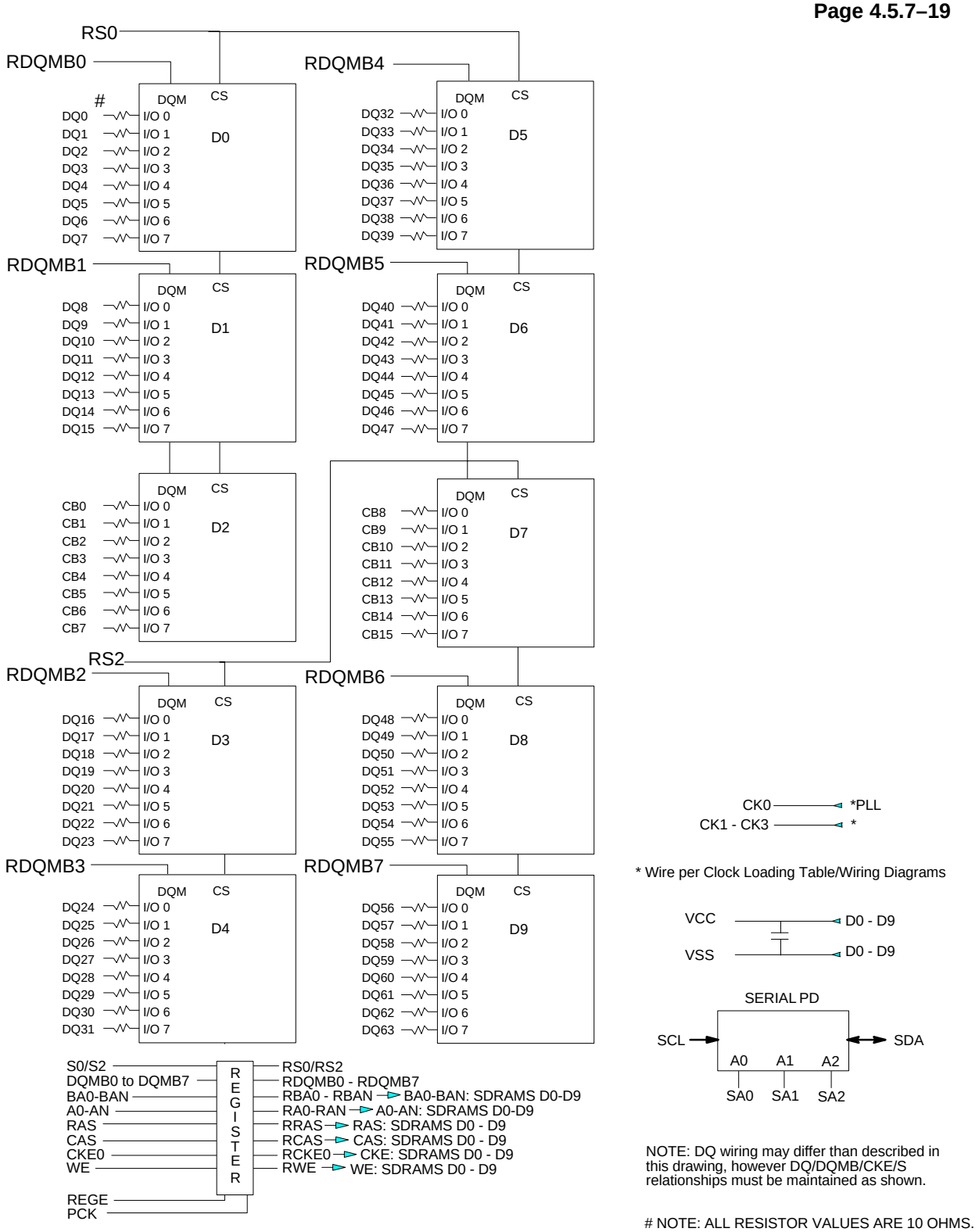
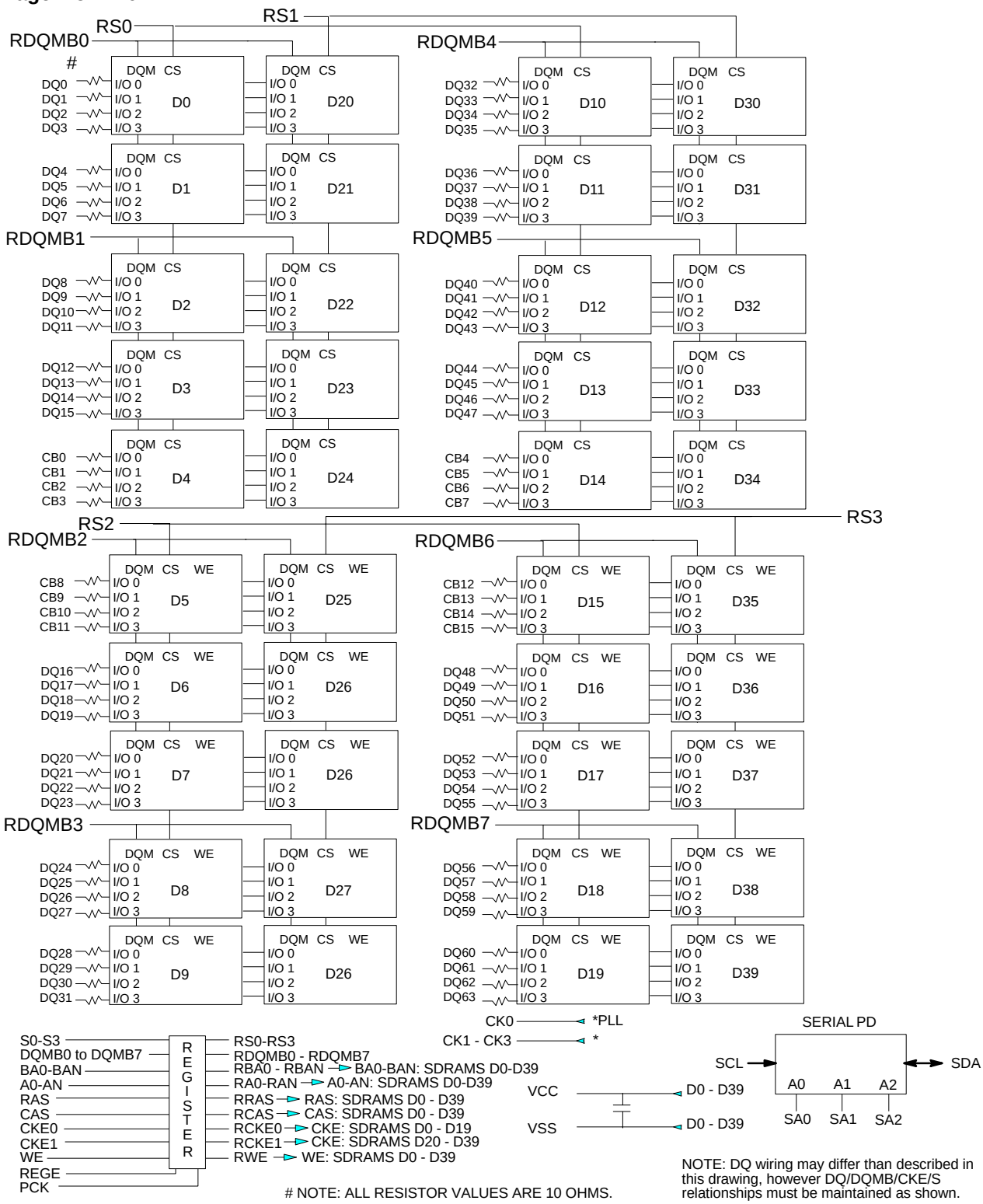


Figure 4.5.7–S
X80 ECC REGISTERED SDRAM DIMM, 1 Bank with X8 SDRAMs



NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.7–T
X80 ECC REGISTERED SDRAM DIMM, 2 Banks with X4 SDRAMs

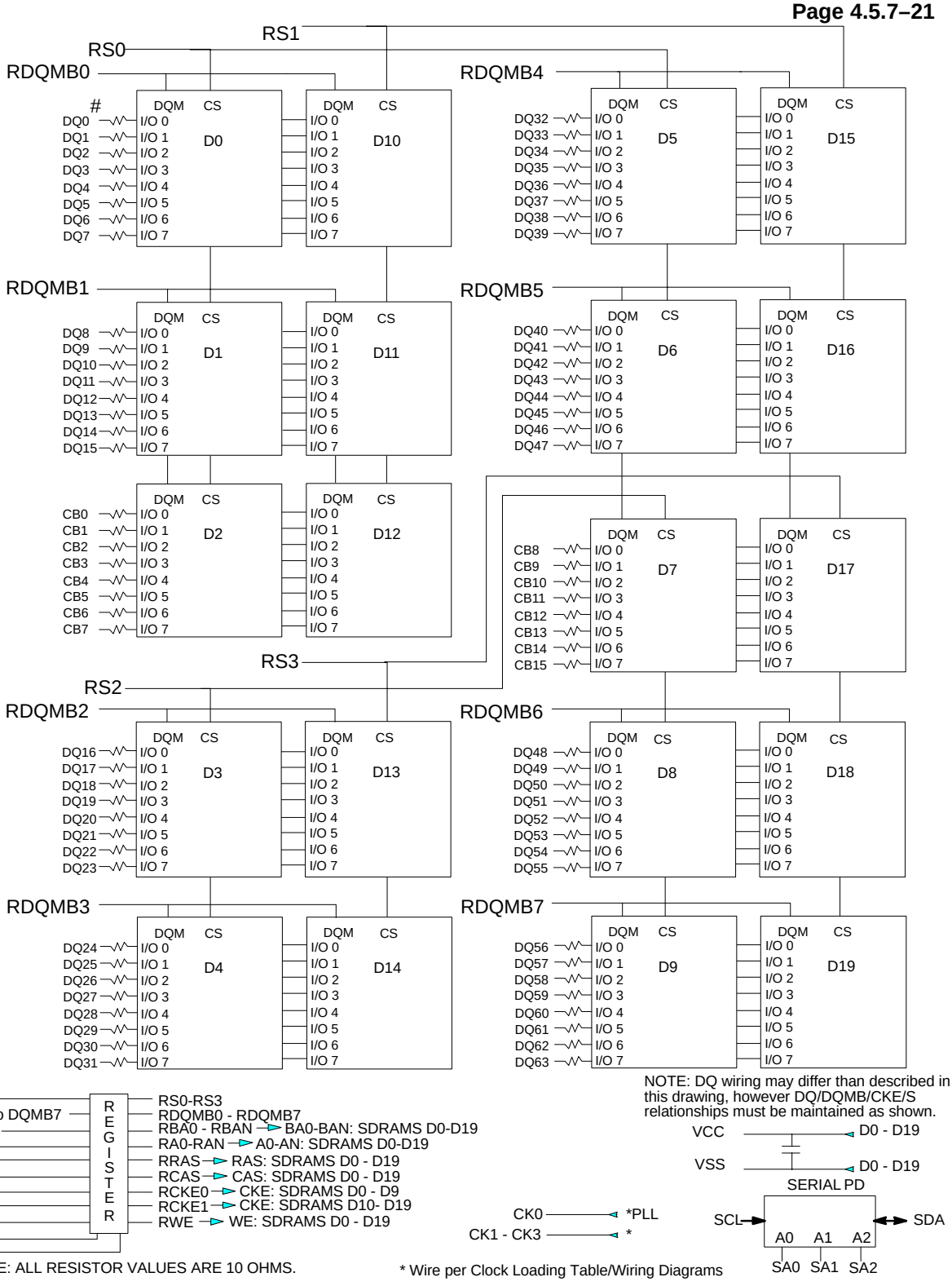
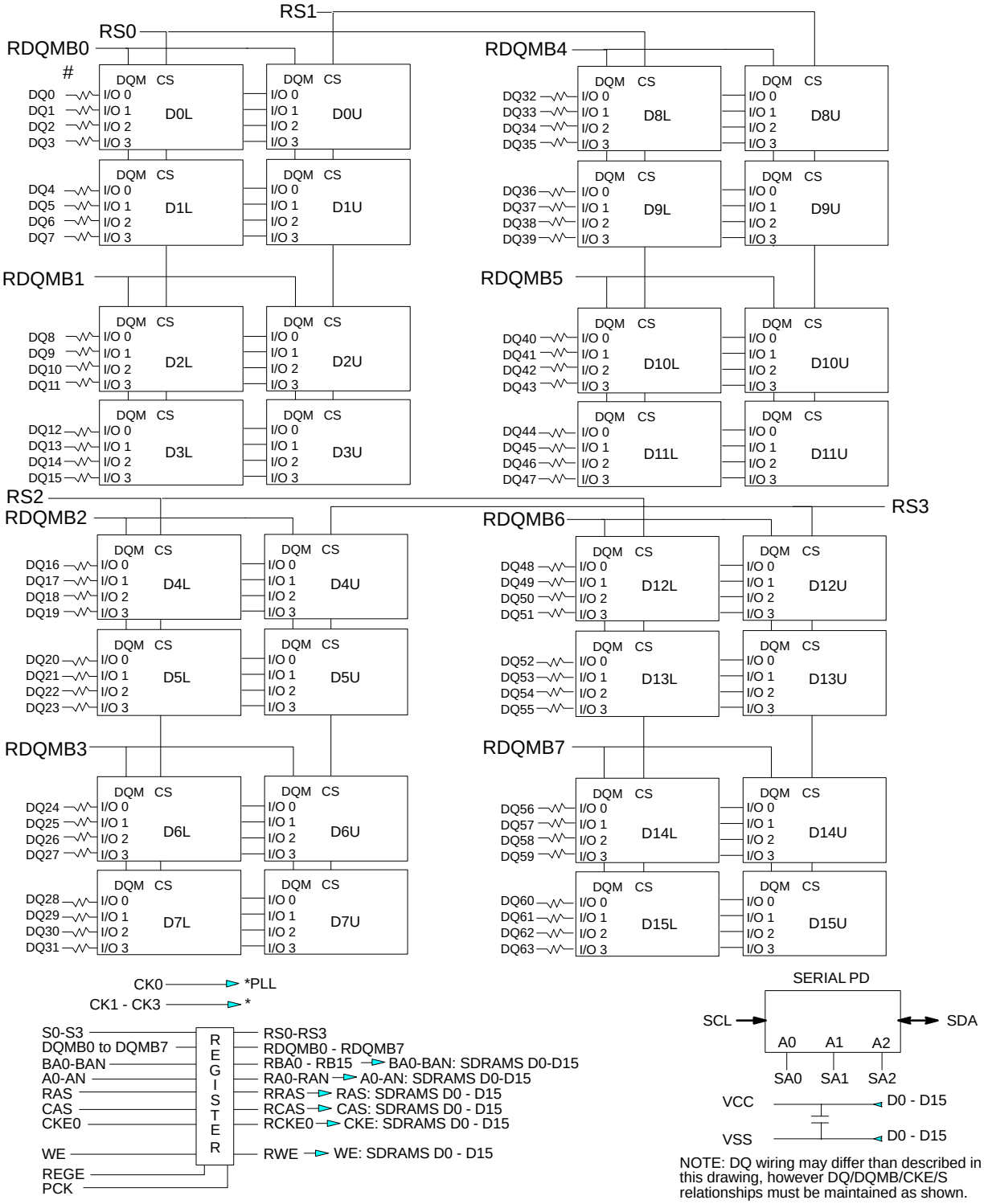


Figure 4.5.7–U
X80 ECC REGISTERED SDRAM DIMM, 2 Banks with X8 SDRAMs



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

Figure 4.5.7–V
X64 REGISTERED SDRAM DIMM, 2 Bank with X4 STACKED SDRAMs AND SINGLE CKE PIN

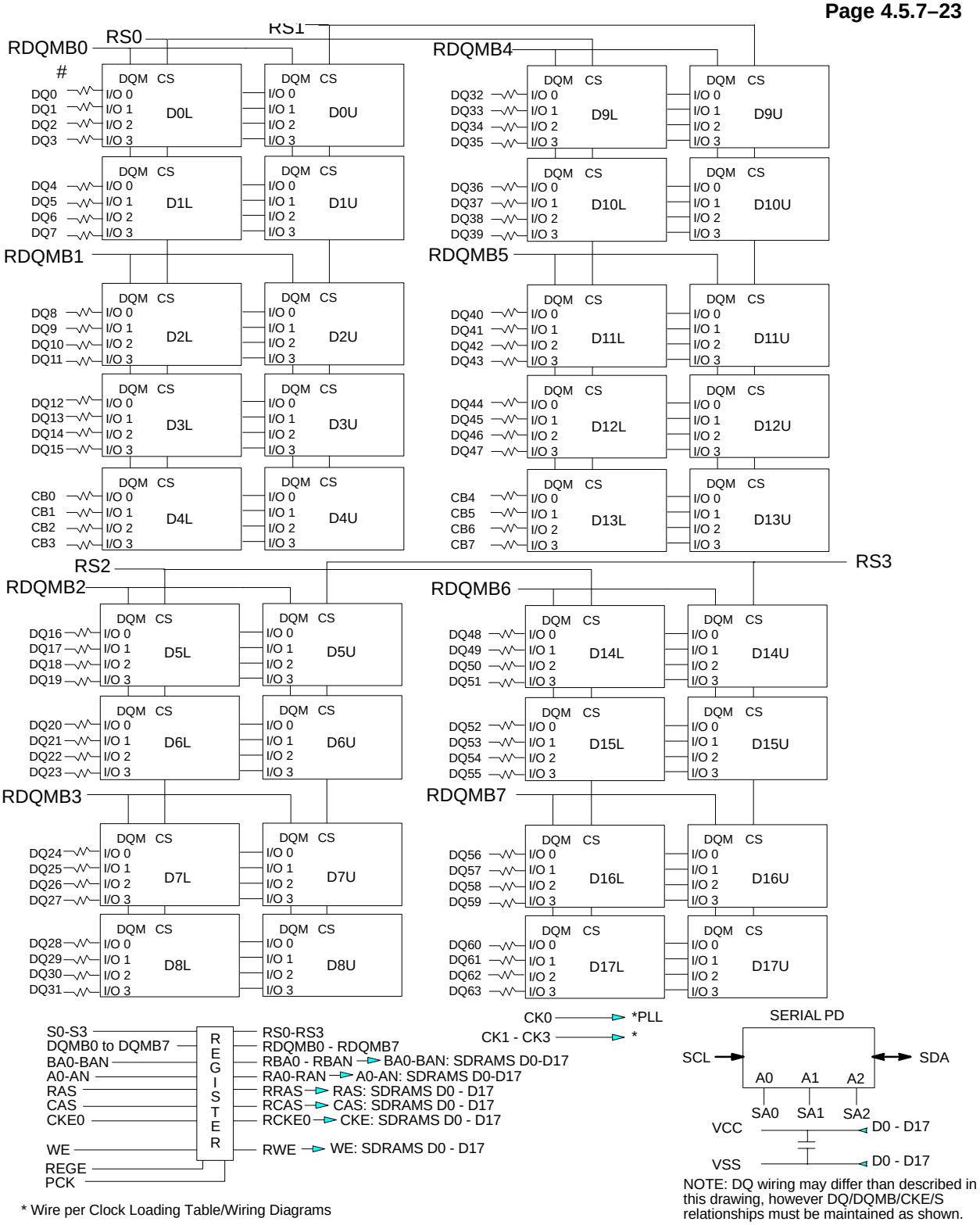


Figure 4.5.7–W
X72 ECC REGISTERED SDRAM DIMM, 2 Bank with X4 STACKED SDRAMs and SINGLE CKE PIN

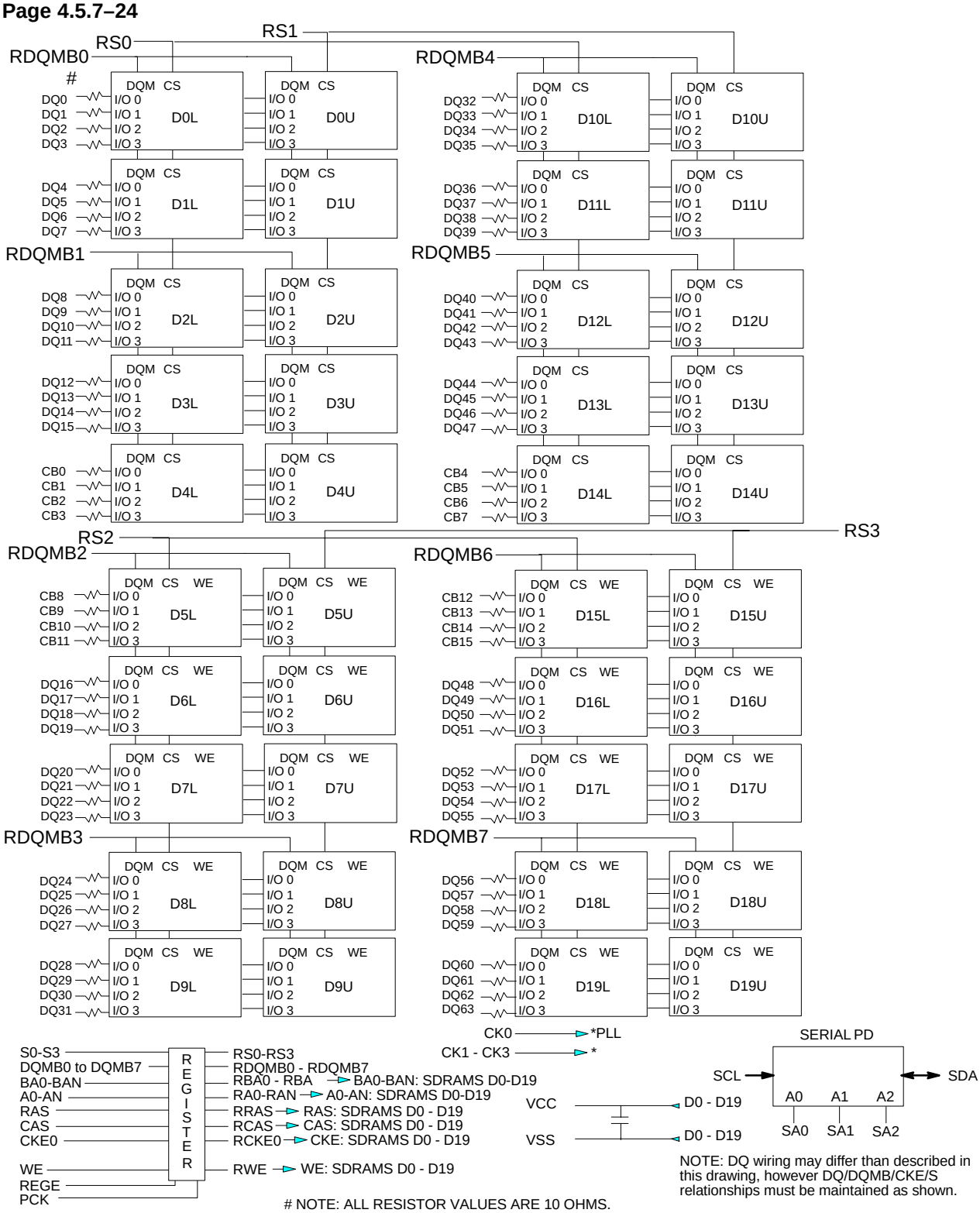


Figure 4.5.7–X
X80 ECC REGISTERED SDRAM DIMM, 2 Bank with X4 STACKED SDRAMs and SINGLE CKE PIN